UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,383	12/20/2001	Jens Leenstra	DE920000098US1	9708

48813 7590 05/16/2006

LAW OFFICE OF IDO TUCHMAN (YOR)
69-60 108 STREET
SUITE 503
FOREST HILLS, NY 11375

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,383	LEENSTRA ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 and new claims 11-16 have been considered. Claims 1, 4, 5, 6, and 10 have been amended as per Applicant's request. New claims 11-16 have been added as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 02 March 2006.

Double Patenting

3. Applicant is advised that should claim 6 be found allowable, claim 10 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k). Claims 6 and 10 have the exact same limitations and their differences are only found in the preamble of the claims. Claim 10's "a computer system having an out-of-order processing system" is encompassed in scope of claim 6's "a processing system having means for executing", since "a processing system" encompasses "a computer system having an out-of-order processing system" in its scope. Also, the preamble of a claim is not generally given patentable weight.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung, U.S. Patent Number 5,778,248 (herein referred to as Leung) in view of Garg et al., U.S. Patent No. 5,974,526 (herein referred to as Garg).

6. Referring to claim 1, Leung has taught a method for operating a processor comprised of an instruction pipeline, the method comprising the steps of:

a. For detection of a dependency, determining for each current instruction that a logic target address of one or more instructions is not the same as a logic source address of said current instruction, said one or more instructions being stored in a temporary buffer associated with a pipeline process downstream of the current instruction (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4);

b. Generating a no-dependency signal associated with said current instruction (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4);

c. Bypassing a portion of the instruction pipeline for the current instruction if the no-dependency signal is active (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4). In regards to Leung, the W stage, i.e. stage that writes to the registers, is bypassed to send the results back into the pipeline faster.

7. Leung has not taught out-of-order processing and a renaming process and addressing a mapping-table-entry with a logical source register address of said current instruction thus determining the mapped physical target register address. Garg has taught out-of-order processing (Garg column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 12, lines 30-58; Figure 1; and Figure 8) and a renaming process and addressing a mapping-table-entry with a logical source register address of said current instruction thus determining the mapped physical target register address (Garg column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 12, lines 30-58; Figure 1; and Figure 8). A person of ordinary skill in the art at the time the invention was made would have recognized that Garg's table allows for tracking of values to the renamed registers (Garg column 4, lines 33-40), thereby ensuring that the values are correctly mapped and can be written to the physical registers correctly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the table of Garg in the device of Leung to ensure correct mapping of values to renamed registers and correct data being written into the physical registers.

8. Referring to claim 2, Leung in view of Garg has taught

a. Comparing a plurality of logic target register addresses and the logic source register address of the current instruction (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4);

b. In case the logic target register addresses and the logic source register address match, setting the no-dependency signal to not active (Leung Abstract; column 1,

lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4); and

c. Generating a dependency signal for the respective source register (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4).

9. Referring to claim 3, Leung in view of Garg has taught evaluating 'valid'-bits of speculative target registers stored in a storage associated with speculatively calculated instruction result data to generate the no-dependency signal (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4).

10. Referring to claims 4 and 5, Leung in view of Garg has taught

a. Reading a committed-status flag in said entry (Garg column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 12, lines 30-58; Figure 1; and Figure 8);

b. Comparing the logic target register address and the logic source register address of the current instruction (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4);

c. In case the logic target register addresses and the logic source register address match, setting the no-dependency signal to not active (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4); and

d. Generating a dependency signal for the respective source register (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4).

11. Referring to claim 6, Gaertner has taught a processing system having means for executing a readable machine language, said readable machine language comprises:

a. A first computer readable code embodied in tangible media for, the detection of a dependency, determining for each current instruction that a logic target address of one or more instructions stored in a temporary buffer associated with a pipeline process downstream of the current instruction is not the same as a logic source address of said current instruction (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4),

b. A second computer readable code embodied in tangible media for generating a no-dependency signal associated with said current instruction (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4), and

c. A third computer readable code embodied in tangible media for bypassing a portion of the instruction pipeline for the current instruction is the no-dependency signal is active (Leung Abstract; column 1, lines 5-40; column 1, line 66 to column 2, line 31; column 3, lines 11-25 and 55-64; column 4, lines 20-49; Figure 2; Figure 3; and Figure 4).

12. Leung has not taught out-of-order processing and a renaming process (Garg column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 12, lines 30-58; Figure 1; and Figure 8). A person of ordinary skill in the art at the time the invention was made would have recognized that Garg's table allows for tracking of values to the renamed registers (Garg column 4, lines 33-40), thereby ensuring that the values are correctly mapped and can be written to the physical registers correctly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the table of Garg in the device of Leung to ensure correct mapping of values to renamed registers and correct data being written into the physical registers.

13. Referring to claims 7-9, Leung in view of Garg has taught

a. In case of a content-addressable memory (CAM)-based renaming scheme (see Garg, Co1.8 lines 38-65 and Col. 12 lines 42-58) the first computer readable code for determining the dependency of a current instruction comprises a compare logic in which all instructions to be checked for dependency are involved and a post-connected OR gate (see Garg, 206 of Fig.2 and 700 of Fig.7). Here, each generic comparison block (see Garg, 204 of Fig.2) performs three separate comparisons on a current and prior instructions operands (see Garg, Fig.7), and the generic comparison block outputs that a dependency exists if any of the three individual comparisons are true (see Garg, Col. 10 line 56 - Col. 11 line 46). Further, the mapping-table based renaming system used by Garg (see Garg, Col.8 lines 38-65 and Col. 12 lines 42-58) is also inherently content-addressable, as it is indexed into using contents of its registers (see Garg, Col. 12 lines 42-58).

b. A plurality of AND gates (see Garg, 808 of Fig.8) the input of which comprises the target register ("valid-bits" signal (see Garg, 512/514 of Fig.5 and Col. 10 lines 56-61) and a respective compare logic output signal (see Garg, Figs. 2, 7 and 8). Here, there is a plurality of A'ND gates (see Garg, 808 of Fig.8) because the circuit of Fig.8 is duplicated three times in comparators 702, 704 and 706, as well as many times in the Data Dependency Checker (see Garg, Fig.2 and Col. 10 line 56 - Col. 11 line 46).

14. Referring to claims 11 and 13, Leung in view of Garg has taught, taking claim 11 as exemplary, the method according to claim 1, further comprising partitioning the current instruction into a reorder buffer and an architectural register array, the reorder buffer configured to store speculative results of the current instruction and the architectural register array configured to store an architectural state of the processor (Garg column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 8, lines 41-50; column 12, lines 30-58; Figure 1; and Figure 8). Claim 13 is substantially similar to claim 11 and is rejected for similar reasons.

15. Referring to claims 12 and 14, Leung in view of Garg has taught, taking claim 12 as exemplary, the method according to claim 11 wherein the no-dependency signal is logically ANDed with a plurality of validity bits indicating data is available at the reorder buffer and the architectural register array (Garg, 808 of Fig.8 and Figs. 2 and 8). Here, there is a plurality of A'ND gates (see Garg, 808 of Fig.8) because the circuit of Fig.8 is duplicated three times in comparators 702, 704 and 706, as well as many times in the Data Dependency Checker (see

Garg, Fig.2 and Col. 10 line 56 - Col. 11 line 46). Claim 14 is substantially similar to claim 12 and is rejected for similar reasons.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaertner et al., U.S. Patent Number 5,996,063 (herein referred to as Gaertner) in view of Garg et al., U.S. Patent No. 5,974,526 (herein referred to as Garg). Gaertner has taught a computer system having an out-of-order processing system, said computer system executes a readable machine language (Applicant's claim 10), said readable machine language comprises:

a. A first computer readable code for, the detection of a dependency, determining for each current instruction involved in a renaming process that a logic target address of one or more instructions stored in a temporary buffer associated with a pipeline process downstream of the current instruction is not the same as a logic source address of said current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4),

b. A second computer readable code for generating a no-dependency signal associated with said current instruction (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4),

c. A third computer readable code for assigning an entry in the temporary buffer to the logic source address of said current instruction if the no-dependency signal is not active (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4), and

d. A fourth computer readable code for issuing the instruction operand data to an instruction execution unit without assigning the entry in the temporary buffer to

the logic source address of said current instruction if the no-dependency signal is active (Gaertner column 8, lines 6-54; Figure 2; Figure 3; and Figure 4).

17. Gaertner has not taught a fifth readable code embodied in tangible media for addressing a mapping-table-entry with a logical source register address of said current instruction thus determining the mapped physical target register address. Garg has taught out-of-order processing (Garg column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 12, lines 30-58; Figure 1; and Figure 8) and a renaming process and addressing a mapping-table-entry with a logical source register address of said current instruction thus determining the mapped physical target register address(Garg column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 12, lines 30-58; Figure 1; and Figure 8). A person of ordinary skill in the art at the time the invention was made would have recognized that Garg's table allows for tracking of values to the renamed registers (Garg column 4, lines 33-40), thereby ensuring that the values are correctly mapped and can be written to the physical registers correctly. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the table of Garg in the device of Leung to ensure correct mapping of values to renamed registers and correct data being written into the physical registers.

18. Referring to claim 15, Gaertner in view of Garg has taught the computer system according to claim 10, further comprising a sixth computer readable code embodied in tangible media for partitioning the current instruction into a reorder buffer and an architectural register array, the reorder buffer configured to store speculative results of the current instruction and the architectural register array configured to store an architectural state of the processor (Garg

column 1, line 66 to column 2, line 15; column 3, lines 11-27; column 4, lines 17-40; column 6, lines 48-63; column 8, lines 41-50; column 12, lines 30-58; Figure 1; and Figure 8).

19. Referring to claim 16, Gaertner in view of Garg has taught the computer system according to claim 15, wherein the no-dependency signal is logically ANDed with a plurality of validity bits indicating data is available at the reorder buffer and the architectural register array. (Garg, 808 of Fig.8 and Figs. 2 and 8). Here, there is a plurality of AND gates (see Garg, 808 of Fig.8) because the circuit of Fig.8 is duplicated three times in comparators 702, 704 and 706, as well as many times in the Data Dependency Checker (see Garg, Fig.2 and Col. 10 line 56 - Col. 11 line 46). Claim 14 is substantially similar to claim 12 and is rejected for similar reasons.

Response to Arguments

20. Applicant's arguments filed 02 March 2006 have been fully considered but they are not persuasive. Applicant argues in essence on pages 7-11

> The Applicants...submit...Garg do no teach or suggest addressing a mapping-table-entry of a mapping table with a logical source register address of said current instruction thus determining the mapped physical target register address. Furthermore, Leung does not teach or suggest a renaming process.

21. This has not been found persuasive. The passages cited were not meant to individually show this limitation but the combination of the passages showed this limitation. For example, Garg has taught in column 3, line 11 to column 4, line 40 has taught that register renaming maps a logical register to a physical register, so the final value is mapped to the correct physical register. This mapping is identified by the logical register address and, since it is mapped to a physical register, there must be some type of data element containing the mapping, e.g. a

mapping table. For more information on register renaming, please see John Kubiatowicz's "CS252 Graduate Computer Architecture Lecture7 Reorder Buffers and Explicit Register Renaming" ©September 2000 slides 7.24-7.55; Moudgill, Pingali, and Vassiliadis's "Register Renaming and Dynamic Speculation: an Alternative Approach" IEEE ©1993; and Gonzalez, Gonzalez, and Valero's "Virtual-Physical Registers" IEEE ©1998.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
12 May 2006

ERIC COLEMAN
PRIMARY EXAMINER